

Fonctions logiques (Portes logiques)

ET (esperluette)

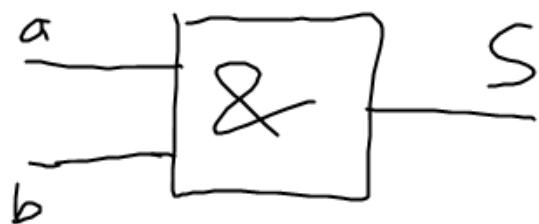


Table de vérité:

a	b	S
0	0	0
0	1	0
1	0	0
1	1	1

Arduino: &&

Equation: $S = a \cdot b$

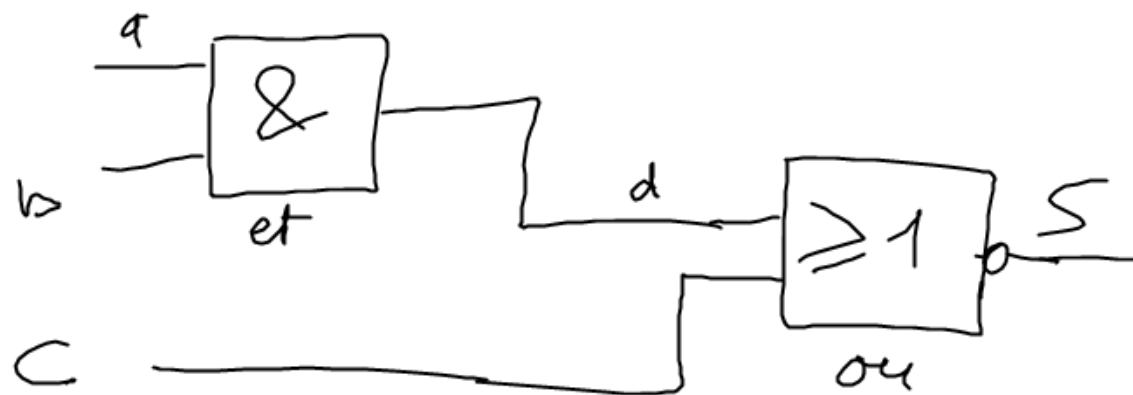
OU



a	b	S
0	0	0
0	1	1
1	0	1
1	1	1

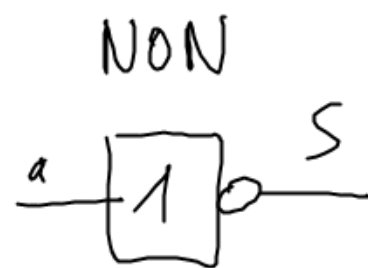
Arduino: || (2x grep)

Equation: $S = a + b$



a	b	c	S
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$\begin{aligned}
 S &= \overline{a \cdot b + c} \\
 &= \overline{a \cdot b} \cdot \overline{c} \\
 &= (\overline{a} + \overline{b}) \cdot \overline{c}
 \end{aligned}$$



a	S
0	1
1	0

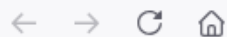
$$S = \overline{a}$$

$$\begin{aligned}
 S &= a(b+c) = ab+ac \\
 S &= a + b \cdot c = (a+b) \cdot (a+c)
 \end{aligned}$$

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principaux théorèmes et propriétés sont rappelés dans le tableau suivant :

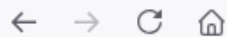
Propriétés / théorèmes	Equations logiques
Commutativité	$a + b = b + a$ $a \cdot b = b \cdot a$
Associativité	$(a + b) + c = a + (b + c)$ $(a \cdot b) \cdot c = a \cdot (b \cdot c)$
Distributivité	$a \cdot (b + c) = (a \cdot b) + (a \cdot c)$ $a + (b \cdot c) = (a + b) \cdot (a + c)$
Eléments neutres Théorème des bornes universelles	$a + 0 = a$ $a \cdot 1 = a$
Complémentation Théorème de non contradiction	$a + \bar{a} = 1$ $a \cdot \bar{a} = 0$
Théorème d'impotence	$a + a = a$ $a \cdot a = a$
Eléments absorbants Théorème du tiers exclus	$a + 1 = 1$ $a \cdot 0 = 0$
Théorème d'absorption	$a + (a \cdot b) = a$ $a \cdot (a + b) = a$
Théorème d'involution	$\overline{(\bar{a})} = a$ $\overline{(\overline{\bar{a}})} = \bar{a}$
Théorème d'inclusion	$a \cdot b + a \cdot \bar{b} = a$


<https://tiplanet.org/modules/archives/downloads2/1446669631.66104/page0m.png>


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Opérateur	équation logique	symbole AFNOR	symbole ASGS	table de vérité	schéma à contact															
OUI	$S = a$			<table><tr><td>a</td><td>S</td></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	a	S	0	0	1	1										
a	S																			
0	0																			
1	1																			
NON	$S = \bar{a}$			<table><tr><td>a</td><td>S</td></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	a	S	0	1	1	0										
a	S																			
0	1																			
1	0																			
OU	$S = a + b$			<table><tr><td>a</td><td>b</td><td>S</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	a	b	S	0	0	0	0	1	1	1	0	1	1	1	1	
a	b	S																		
0	0	0																		
0	1	1																		
1	0	1																		
1	1	1																		
ET	$S = a.b$			<table><tr><td>a</td><td>b</td><td>S</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	a	b	S	0	0	0	0	1	0	1	0	0	1	1	1	
a	b	S																		
0	0	0																		
0	1	0																		
1	0	0																		
1	1	1																		
INHIBITION	$S = \bar{a}.b$			<table><tr><td>a</td><td>b</td><td>S</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	a	b	S	0	0	0	0	1	1	1	0	0	1	1	0	
a	b	S																		
0	0	0																		
0	1	1																		
1	0	0																		
1	1	0																		
NAND (NON ET)	$S = \overline{a.b} = \bar{a} + \bar{b}$			<table><tr><td>a</td><td>b</td><td>S</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	a	b	S	0	0	1	0	1	1	1	0	1	1	1	0	
a	b	S																		
0	0	1																		
0	1	1																		
1	0	1																		
1	1	0																		
NOR (NON OU)	$S = \overline{a + b} = \bar{a}.\bar{b}$			<table><tr><td>a</td><td>b</td><td>S</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	a	b	S	0	0	1	0	1	0	1	0	0	1	1	0	
a	b	S																		
0	0	1																		
0	1	0																		
1	0	0																		
1	1	0																		
OU EXCLUSIF	$S = a \oplus b$			<table><tr><td>a</td><td>b</td><td>S</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	a	b	S	0	0	0	0	1	1	1	0	1	1	1	0	
a	b	S																		
0	0	0																		
0	1	1																		
1	0	1																		
1	1	0																		
IDENTITE	$S = \overline{a \oplus b}$			<table><tr><td>a</td><td>b</td><td>S</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	a	b	S	0	0	1	0	1	0	1	0	0	1	1	1	
a	b	S																		
0	0	1																		
0	1	0																		
1	0	0																		
1	1	1																		



74HC05



Connexion

Diodes Incorporated 74HC05 Série Onduleurs

Onduleurs HEX INVERTERS 2-6V 4mA at VCC 4.5V. Diodes Incorporated 74HC05T14-13.

74HC05T14-13; Diodes Incorporated; 1: 0,58 €; 2 765En stock.

Images :



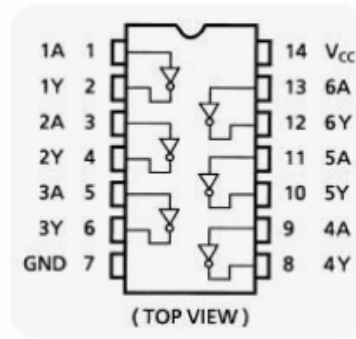
74HC05 Datasheet(PDF) - ST...

ALLDATASHEET.COM



7400 Series Guide: 74HC05/7...

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74HC05 Datasheet PDF , Tosh...

DATASHEETBANK.COM

Afficher plus d'images ▼



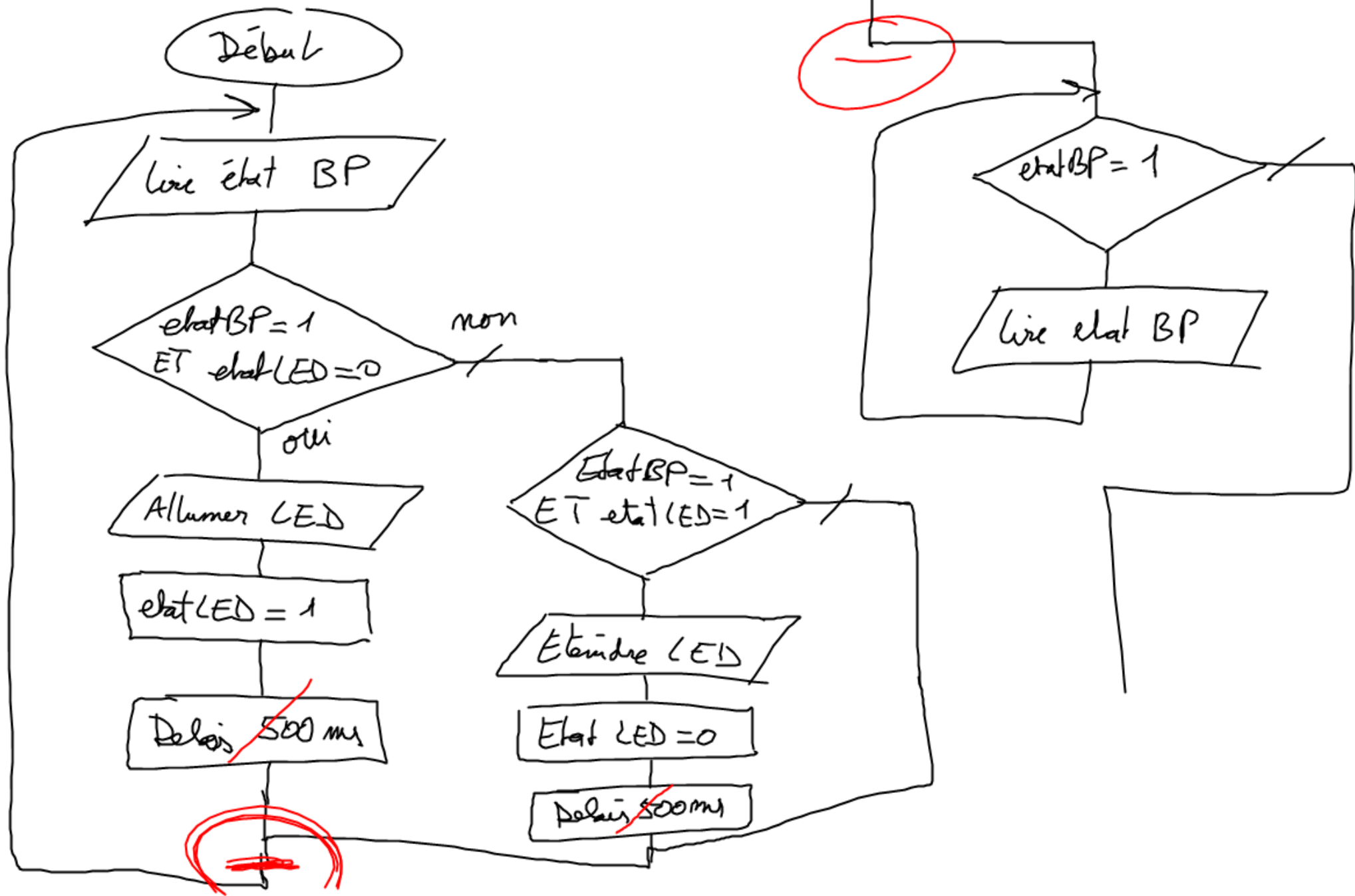
composant-electronique.fr

<https://composant-electronique.fr/circuit-integre-logiqu...>

Circuit intégré logique 74HC05. Avtronic

Circuit intégré logique 74HC05 HEX INVERTER OPEN COLLECTOR. Constructeur:







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sketch_mar07a \$

```
void setup() {  
  pinMode(pinBP, INPUT);  
  pinMode(pinLED, OUTPUT);  
}  
  
void loop() {  
  etatBP = digitalRead(pinBP);  
  if (etatBP == 1 && etatLED == 0) {  
    digitalWrite(pinLED, 1);  
    etatLED = 1;  
  }  
  else if (etatBP == 1 && etatLED == 1) {  
    digitalWrite(pinLED, 0);  
    etatLED = 0;  
  }  
  while (etatBP == 1) {  
    etatBP = digitalRead(pinBP);  
  }  
}
```

Formatage automatique terminé.

